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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/901,295	07/09/2001	Tetsuya Yano	FUJR 18.797	8755

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EXAMINER	
BAKER, STEPHEN M	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/901,295	YANO ET AL.	
	Examiner	Art Unit	
	Stephen M. Baker	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-14 and 16-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-14 and 16-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 2, 4-14 and 16-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1: an essential means for interleaving and deinterleaving inputs and outputs of the decoders is omitted; in lines 1-2, "for iteratively decoding received signals a set number of times" is confusing and apparently should be "for iteratively decoding received signals up to a set number of times" as lines 12-14 contradictorily recite "halting the decoding ... even if the number of times decoding has been performed has not attained said set number of times" as the only way of halting decoding; "results" of each elementary decoder are described as being used by the other elementary decoder without mention of interleaving or deinterleaving, presumably requiring the elementary decoders to include interleaving and deinterleaving within their decoding processing, in contradiction to the terminology of the disclosure.

Regarding claim 2: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; an essential means for decoding is omitted; in lines 1-2, "for iteratively decoding a received signal a set number of times" is confusing and apparently should be "for iteratively decoding a received signal" as lines 6-7 recite

"halting the decoding operation even if number (sic) of times decoding has been performed has not attained (sic) said set number of times" and lines 9-10 recite another exception wherein the "set number of times" is exceeded; in lines 6-7, "even if number of times decoding has been performed has not attained said set number of times" is awkward and apparently should be "even if the number of times decoding has been performed is not a set number of times"; in line 9, "when decoding has been performed" is confusing and apparently should be "after decoding has been performed".

Regarding claim 4: "results" of each elementary decoder are described as being used by the other elementary decoder without mention of interleaving or deinterleaving, presumably requiring the elementary decoders to include interleaving and deinterleaving within their decoding processing, in contradiction to the terminology of the disclosure, whereas lines 15-16 apparently require an elementary decoder to not include interleaving or deinterleaving within its decoding processing.

Regarding claim 5: in lines 5-10, "results" of the elementary decoder are described as being used without mention of interleaving or deinterleaving, presumably requiring the elementary decoder to include interleaving and deinterleaving within its decoding processing, in contradiction to the terminology of the disclosure, and, in line 11, "interleaving the received signal ... and inputting the same" implies that the "received signal" can be called the same thing whether it is interleaved or not, whereas line 19 apparently contradictorily attempts to draw a distinction between a signal and its interleaved or deinterleaved version.

Regarding claim 6: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; "results" of each elementary decoder are described as being used by the other elementary decoder without mention of interleaving or deinterleaving, in contradiction to the terminology of the disclosure; in line 9, "first and second" is needlessly confusing and apparently should be "first or second".

Regarding claim 7: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; "results" of each elementary decoder are described as being used by the other elementary decoder without mention of interleaving or deinterleaving, in contradiction to the terminology of the disclosure; the comma in line 9 serves no apparent purpose.

Regarding claims 8 and 14: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; "results" of each elementary decoder are described as being used by the other elementary decoder without mention of interleaving or deinterleaving, in contradiction to the terminology of the disclosure.

Regarding claim 9: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; an essential means for decoding is omitted.

Regarding claims 10 and 11: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; an essential means for decoding is omitted; "results" of the elementary decoder are described as being used without mention of interleaving or deinterleaving, presumably requiring the elementary

decoder to include interleaving and deinterleaving within their decoding processing, in contradiction to the terminology of the disclosure.

Regarding claim 13: the presumption of requiring the elementary decoder to include interleaving and deinterleaving within their decoding processing, as apparently called for by claim 11, is apparently contradicted.

Regarding claim 16: an essential process of interleaving is apparently omitted from the description of the decoder function.

Regarding claims 17 and 20: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; an essential means for decoding is omitted.

Regarding claims 21 and 22: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted.

Regarding claim 23: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted; an essential means for decoding is omitted; "results" of the elementary decoder are described as being used without mention of interleaving or deinterleaving, presumably requiring the elementary decoder to include interleaving and deinterleaving within their decoding processing, in contradiction to the terminology of the disclosure.

Regarding claim 24: an essential means for interleaving and deinterleaving inputs and outputs of the decoding is omitted.

Claim Rejections - 35 USC § 102

3. Claims 4, 11, 13, 14 and 16-24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,192,503 to Chennakeshu *et al* (hereafter Chennakeshu).

Regarding claim 4, Chennakeshu shows (FIG. 5) a "turbo decoder" comprising "first and second elementary decoders" (252a, 252b) which include interleaving and deinterleaving means (col. 9, lines 27+) necessary to decode the output of a parallel concatenated convolutional code encoder (FIG. 2), thereby teaching an "interleaving unit" and a "deinterleaving unit". Furthermore, Chennakeshu teaches that the first iteration may begin with either the first decoder processing or the second decoder processing (col. 9, lines 45+) in accordance with the relative strengths of the received first encoder bits or second encoder bits. Consequently, Chennakeshu teaches beginning decoding using the second encoder output and thus with a "first decoding processing using received signals ya and yc" where "ya" represents the "first data" *i.e.* the systematic bits, and yc represents the second encoding's output "obtained by interleaving and then encoding first data".

Regarding claims 11 and 13, Chennakeshu's teaching of interleaving and deinterleaving means (col. 9, lines 27+) necessary to decode the output of a parallel concatenated convolutional code encoder requires a "memory for storing the results of the first decoding processing" so the results can be reordered as required by the second decoding processing, and Chennakeshu's teaching of selecting which decoding is to be performed first indicates the "first decoding processing" results require deinterleaving

before output to the error detector in a situation where the interleaved component code is decoded first. Accordingly, Chennakeshu teaches "outputting the results of the first decoding processing stored in said memory in accordance with the result of error detection", wherein "said memory" is a deinterleaving memory of the interleaved code decoder when selected for the "first decoding processing" of the iterative decoding.

Regarding claims 14, 21, 22 and 24, Chennakeshu's two component code decoders (252a, 252b) can be considered to collectively provide "a decoder for executing the first and second decoding processing".

Regarding claims 16, 19 and 24, as Chennakeshu teaches selecting the output of either component code decoder for providing output as the corrected data (col. 10, lines 35+), as Chennakeshu's error detector presumably operates on non-interleaved data because the error correction coding (102) is performed on non-interleaved data, and as the output of the decoder of the non-interleaved code only requires interleaving for processing by the decoder of the interleaved code, it is apparent that Chennakeshu teaches "output means for outputting the results of the first decoding processing ... as a decoded result of the turbo decoder directly without intervention of interleaving or deinterleaving".

Regarding claim 17 and further regarding claim 22, as is apparent from the above discussion, Chennakeshu's error detector (254) serves as a "selector for selecting and outputting one of the results of the first and second decoding processing" or a "controller" for same.

Regarding claim 18, as Chennakeshu's error detector presumably operates on non-interleaved data because the error correction coding (102) is performed on non-interleaved data, and as the output of the decoder of the interleaved code requires deinterleaving to return the order of data to that encoded by the error detection code, Chennakeshu's decoding arrangement apparently can operate such that "said selector selects and outputs a signal obtained by deinterleaving the results of the second decoding processing as a decoding output of the turbo decoder".

Regarding claims 20 and 23, and further regarding claim 21, as Chennakeshu teaches that the first iteration may begin with either the first decoder processing or the second decoder processing (col. 9, lines 45+) , Chennakeshu teaches "a controller for changing an order of the first and second decoding processing".

4. Claims 5 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,122,763 to Pyndiah *et al* (hereafter Pyndiah).

Pyndiah shows a "turbo decoder" (Fig. 6) for a product code created from "first data" and having row and column parities respectively serving as "second data yb obtained by encoding said first data" and "third data yc obtained by interleaving and then encoding said first data", assuming the data to be encoded is originally in row order. Pyndiah's decoder has "one elementary decoder" (65) and a memory (67) serving as an "interleaving unit". A processor controls the reading and writing of the memory (67), serving as a "selection circuit for selecting the signal yc when the first decoding processing is executed, selecting the signal yb when the second decoding processing is executed, and inputting the selected signal to the elementary decoder", as

well as a "means for deinterleaving results of the first decoding processing, interleaving results of the second decoding processing and inputting the deinterleaved and interleaved results to the elementary decoder". As interleaving and deinterleaving are performed upon reading from the memory (67) rather than upon outputting data from the "elementary decoder" (65), "results of decoding are output from said elementary directly without intervention of interleaving or deinterleaving".

Regarding claim 8, as reordering the data for decoding changes the pattern of remaining errors in the data as ordered, it can be said that "the nature of an error generation pattern in decoded data is controlled by switching the received signals input to the elementary decoder at the timings of the first and second decoding processing".

5. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by the published article "Illuminating the Structure of Code and Decoder of Parallel Concatenated Recursive Systematic (Turbo) Codes" by Robertson (hereafter Robertson).

6. Robertson discloses a turbo decoder (FIG. 1) including two MAP decoders ("MAP 1", "MAP 2") for "iterative decoding processing" an "error detector" ("Estimate m_2L Evaluate σ^{2}") for "detecting errors in results of previous decoding in parallel with a current decoding operation in the iterative decoding processing", and a "controller" ("Threshold ($\sigma^2 < 0.03$)", "Decision and De-Interleaver") that "when absence of error has been detected in the results of the previous decoding, is operable for outputting the results of the previous decoding and halting the current decoding operation even if a number of times decoding has been performed has not attained a set number of times",

considering the "current decoding operation" to include the operation of the deinterleaver (between MAP 1 and MAP 2) in combination with the MAP 1 decoder.

7. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,292,918 to Sindhushayana *et al* (hereafter Sindhushayana).

Sindhushayana discloses a turbo decoder including a means (70) for "executing first decoding processing using a first set of signals including a first received signal selected from among received signals" and a means (68) for "executing second decoding processing using a second set of signals including a second received signal selected from among the received signals", where the "first set of signals" and the "second set of signals" correspond to two different packets. Sindhushayana also shows a CRC checker (83) providing "an error detector for detecting errors in results of the first decoding processing while the second decoding processing is being executed".

Claim Rejections - 35 USC § 103

8. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chennakeshu.

Regarding claim 6, Chennakeshu's error detector (254) serves as a "selection circuit for selecting and outputting the results of first and second decoding processing output from said first and second elementary decoders". As the pattern of remaining errors changes with each decoding, the selection performed by Chennakeshu's error detector (254) is such that "the nature of an error generation pattern in decoded data finally output is controlled by selecting the decoded data to be output".

Regarding claim 7, Chennakeshu's teaching that the first iteration may begin with either the first decoder processing or the second decoder processing (col. 9, lines 45+) in accordance with the relative strengths of the received first encoder bits or second encoder bits requires a "selection circuit for selecting a combination of received signals input to the first elementary decoder ... and selecting a received signal input to the second elementary decoder" operating such that "the nature of an error generation pattern in decoded data is controlled by switching the received signals input to the first and second elementary decoders".

Chennakeshu does not teach limiting the iterations to "a set number of times".

Official Notice is taken that the advantages of limiting the number of iterations in a turbo code decoder were already well known at the time the invention was made, as evidenced by Smith. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to implement Chennakeshu's decoder with a means to limit the maximum number of iterations. Such an implementation would have been obvious because the advantages of limiting the number of iterations in a turbo code decoder were already well known.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 2, 4-14 and 16-24 have been considered but are moot in view of the new grounds of rejection.

Allowable Subject Matter

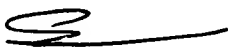
10. Claim 2 would be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen M. Baker whose telephone number is (571) 272-3814. The examiner can normally be reached on Monday-Friday (11:00 AM - 7:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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Art Unit 2133

smb